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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/967,155 | 09/28/2001 | Robert A. Lester | COMP:0233 P01-3623 | 4957 |

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Intellectual Property Administration
Legal Department, M/S 35
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EXAMINER

VU, TRISHA U

ART UNIT

PAPER NUMBER

2112

DATE MAILED: 03/30/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

SL

Office Action Summary

Application No.

09/967,155

Applicant(s)

LESTER ET AL.

Examiner

Trisha U. Vu

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 September 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-13 and 19-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-13 and 19-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☒ Claim(s) 14-18 and 24-29 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 September 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 2.
- 4) ☒ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 1-13 and 19-23, drawn to handling deferred replies at a bus bridge, classified in class 710, subclass 306.
 - II. Claims 14-18 and 24-29, drawn to requests blocking, classified in class 710, subclass 200.

2. The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, each of the inventions I and II has separate utility such as stated above. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with Robert Manware (Reg. No. 48,758) on 03-19-04 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-13 and 19-23. Affirmation of this election must be made by applicant in replying to this Office action. Claims 14-18 and 24-29 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3-7, 9-10, and 19-21 are rejected under 35 U.S.C. 102(e) as being anticipated by Hunsaker (US Pub. No. 2003/0037198).

As to claim 1, Hunsaker teaches a method of processing a request in a computer system, comprising the acts of: (a) initiating a read request from a requesting agent (read request from one of PCI/PCI-X devices 187), the requesting agent residing on a bus (bus 185), wherein the read request has an address corresponding to a memory location (in memory 140); (b) receiving the read request at a processor controller (part of bridge 190 “bridge 190 receives the read request from the PCI/PCI-X devices”); (c) sending the read request from the processor controller to an access controller (Memory controller 130); (d) sending a deferred reply (split response) from the processor controller to the requesting

agent when the processor controller is free to process the read request; (e) delivering data residing at the address corresponding to the memory location to the access controller (Memory controller 130); (f) delivering the data from the access controller to the processor controller (to bridge 190); and (g) delivering the data from the processor (from bridge 190) controller to the requesting agent (Figs. 1-2 and paragraphs [0004], [0023]).

As to claim 3, Hunsaker further teaches act (a) comprises the act of initiating a read request from a processor (processor 110) residing on a processor bus (host bus 120) (Fig. 1).

As to claim 4, Hunsaker further teaches act (a) comprises the act of initiating a read request from a peripheral device (PCI/PCI-X devices 187) residing on an input/output (I/O) bus (bus 185).

As to claim 5, Hunsaker further teaches act (c) comprises the act of sending the request from the processor controller to a memory controller (Memory controller 130) (Figs. 1-2 and paragraphs [0004], [0023]).

As to claim 6, Hunsaker further teaches act (c) comprises the act of sending the request from the processor controller to a tag controller (Memory controller 130 or I/O Controller Hub 150 in part or in combination wherein the I/O Controller Hub 150 may include PCI bus interface, processor interface, interrupt controller, DMA controller, etc...) (Fig. 1 and paragraph [0019]).

As to claim 7, Hunsaker further teaches act (d) comprises the act of sending a deferred reply (split response) immediately upon the agent bus being available to receive data from the memory location (paragraphs [0004], [0023]).

As to claim 9, Hunsaker further teaches acts (d) and (f) are performed simultaneously (paragraphs [0004], [0023]).

As to claim 10, Hunsaker further teaches the acts are performed in the recited order (Figs. 1-2 and paragraphs [0004], [0023]).

As to claim 19, Hunsaker teaches a plurality of buses (buses 185, 195, 120, etc...); a memory system (System Memory 140) operably coupled to the plurality of buses (Fig. 1); and a processor controller (bridge 190, Memory Controller 130, and I/O Controller 150 in part or in combination) coupled to each of the plurality of buses and configured to simultaneously issue a deferred reply (split response) to a requesting device in response to receiving a read request from the requesting device and obtain the data corresponding to the read request from the memory system (Figs. 1-2 and paragraphs [0004], [0022], [0023]).

As to claim 20, Hunsaker further teaches at least one of the plurality of buses comprises a processor bus (host bus 120) (Fig. 1).

As to claim 21, Hunsaker further teaches at least one of the plurality of buses comprises an input/output (I/O) bus (at least bus 185) (Fig. 1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2 and 11-13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunsaker (US Pub. No. 2003/0037198) in view of Solomon (6,647,454).

As to claim 2, the argument above for claim 1 applies. However, Hunsaker does not explicitly disclose sending a data ready signal from the access controller to the processor controller upon receipt of the data at the access controller. Solomon teaches sending a data ready signal (signals a split completion transaction upon obtaining the requested data) from a retrieving interface circuit (bridge 30) to a requesting interface circuit (bridge 20) upon receipt of the data at the retrieving interface circuit (Fig. 3 and col. 3, lines 6-13). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a data ready signal from a retrieving interface circuit to a requesting interface circuit upon receipt of the data at the retrieving interface circuit as taught by Solomon in the system of Hunsaker to give notification of a split transaction to the requesting interface circuit so that it can properly handle the data.

As to claim 11, Hunsaker teaches a method of processing a request in a computer system, comprising the acts of: (a) sending a request from a processor controller (part of bridge 190 "bridge 190 receives the read request from the PCI/PCI-X devices") to an access controller (Memory controller 130) the request originating from an agent; and (b) sending a deferred reply (split response) from the processor controller to the agent after step (a) (Figs. 1-2 and paragraphs [0004], [0023]). However, Hunsaker does not explicitly disclose sending the request is performed in a first clock cycle and sending the deferred reply is performed in a second clock cycle, wherein the second clock cycle being

immediately subsequent to the first clock cycle. Solomon teaches sending the request is performed in a first clock cycle (phase 1) and sending the deferred reply is performed in the second clock cycle subsequent to the first clock cycle (Fig. 2 and col. 2, lines 47-61). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement sending the request is performed in a first clock cycle and sending the deferred reply is performed in a second clock cycle immediately subsequent to the first clock cycle as taught by Solomon in the system of Hunsaker to reduce wait states in processing split requests (col. 1, lines 11-23).

As to claim 12, Hunsaker as modified above further teaches act (a) comprises the act of sending a request from a processor controller to a memory controller (Memory controller 130) on a first clock cycle (Figs. 1-2 and paragraphs [0004], [0023]).

As to claim 13, Hunsaker as modified above further teaches act (a) comprises the act of sending a request for a processor controller to a tag controller (Memory controller 130 or I/O Controller Hub 150 in part or in combination wherein the I/O Controller Hub 150 may include PCI bus interface, processor interface, interrupt controller, DMA controller, etc...) on a first clock cycle (Fig. 1 and paragraph [0019]) on a first clock cycle.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunsaker (US Pub. No. 2003/0037198) and further in view of Ajanovic et al. (5,761,444) (herein after Ajanovic).

As to claim 8, the argument above for claim 1 applies. However, Hunsaker does not explicitly disclose act (d) comprises the act of waiting a predetermined number of clock cycles after the deferred reply is sent before delivering data. Ajanovic teaches waiting a predetermined number of clock cycles after the deferred reply is sent before delivering data (state machine 432 issues a split transaction only when the computer system conditions warrant it) (col. 7, lines 1-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include waiting a predetermined number of clock cycles after the deferred reply is sent before delivering data as taught by Ajanovic in the system of Hunsaker to avoid severe degrade in situations where a penalty is taken unnecessarily.

7. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunsaker (US Pub. No. 2003/0037198) and further in view of Jayakumar et al. (6,012,118) (hereinafter Jayakumar).

As to claim 22, the argument above for claim 19 applies. However, Hunsaker does not explicitly disclose obtaining the data corresponding to the read request from the memory system before issuing a deferred reply to a requesting device. Jayakumar teaches obtaining the data corresponding to the read request before issuing a deferred reply to a requesting device (claim 17 and col. 10, lines 36-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include obtaining the data corresponding to the read request before issuing a deferred reply to a requesting device as taught by Jayakumar in the system of Hunsaker to guarantee that

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data is available at the responding device after issuing the deferred reply and thus reduce the waiting time at the requesting device.

8. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hunsaker (US Pub. No. 2003/0037198) and further in view of Stallmo et al. (5,613,059) (hereinafter Stallmo).

As to claim 23, the argument above for claim 19 applies. However, Hunsaker does not explicitly disclose the memory system comprises a redundant memory system. Stallmo teaches redundant memory system (RAID) (at least col. 1, lines 54-67). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include redundant memory system as taught by Stallmo in the system of Hunsaker to increase the system's fault-tolerance.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses deferred transactions:

US Patent: 5,937,171 Sarangdhar et al.

US Patent 6,073,198 Meyer et al.

US Patent 5,870,567 Hausauer et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

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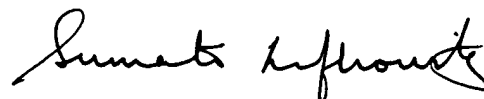
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Trisha U. Vu
Examiner
Art Unit 2112

uv



SUMATI LEFKOWITZ
PRIMARY EXAMINER